Sierra Components, Inc.

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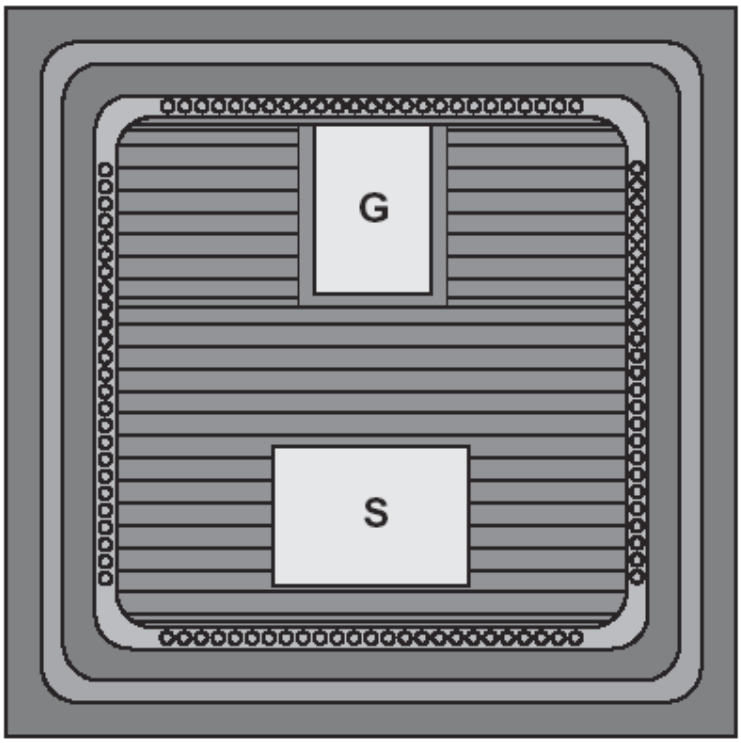
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



Backside: Drain

All dimensions in mils.

Die Geometry	Dimensions			Backside Metal	Bonding Pads[2]		Recommended Assembly Material		
	Length[1]	Width[1]	Thickness		Material	Size	Wire[3]	Wire Size[3]	Preform
VF15	37	37	11 ± 1.5	Au	Al-Cu-Si	4.3 x 5.1	Al or Au	1.3	Epoxy or Au-Si Eutectic

Notes:
1. Maximum values
2. Al-Cu-Si is used for higher operating current densities. Bond pad size represents smaller gate pad.
3. Bond wire size and material depends on AuTCB, TSB or Al USB.

APPROVED BY:	**DIE SIZE : 37 x 37**	**DATE: 5/4/05**
MFG: Supertex	**THICKNESS: 11**	**P/N: VP1550ND**